Non-Destructive Screening Method of Solder Voids in Flip-Chip Package Light-Emitting Diodes Using Thermal Transient Analysis

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1. Introduction

Because of their promising advantages over conventional light sources, light-emitting diodes (LED) have been widely used in many applications such as mobile, display, and lighting. However, the competition among LED companies has been severe due to the excessive supply of the LED products, and a need for cost-reduction has been increased, simultaneously. In order to reduce the cost of the LED packages and to minimize the thermal budget, the chip-on-board (COB) packages and the chip-scale package (CSP) LEDs, based on flip-chip die bonding process, have been developed. Although the flip-chip die bonding process for the COB and CSP LED is useful to the thermal resistance, the precise process control for minimizing voids in solder joint is needed for reliability. In addition, although the in-line screening for bonding failure is very in significance, there is no effective method in the LED industry until now.

2. Methodology

A measurement method for IC and LED package structural integrity has been proposed [1]. This method uses the thermal dynamics, in which the successive junction temperatures of the package have been monitored and analyzed. In order to realize the in-line screening system for bonding failure, measurement time as well as measurement accuracy is very important for throughput. So, we propose a very simple method to discriminate the bonding failure in LED solder joint. The time-constant analysis for the solder joint in the LED packages gives the thermal specific time and we could determine two points of measurement time relating to the thermal specific time. In order to carry out the feasibility test, we made three groups of the LED packages according to the solder joint quality as shown in Fig. 1. LEDs in A group, as a reference, had less than 10% void and had the strength of over 2 kgf in die shear test (DST). On the other hands, B and C groups showed about 50% and 90% voids and strength of over 2 kgf and less than 0.2 kgf in DST, respectively.

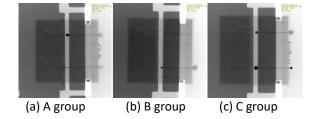
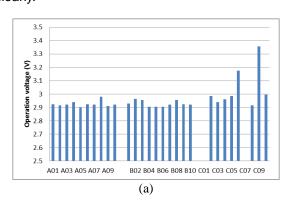


Fig. 1 X-ray of LED chip in A, B, C groups

3. Results

Fig.2. shows the operation voltages and the optical powers of A, B, C LED groups. Operation condition was 350 mA at 25 °C. There was no difference between A and B groups in the operation voltage and the optical power. Although the operation voltages of C group are slightly higher than A group, the optical powers show no difference. Here, we can conclude that the operation voltage and optical power of the LED packages are not appropriate for bonding quality estimation. Since we knew that the thermal specific time for LED chip and flip-chip solder joint of our LED packages is between 0.1 ms and 0.1 s, we could determine the two measurement points of 0.1 ms and 0.1 s. Fig. 3 shows the normalized operation voltages and voltage difference of the LED packages in A, B, C LED groups. Compared to the value of A group, LED packages of B and C groups showed the higher voltage differences clearly.



800
700
(m) 500
100
0
A1 A3 A5 A7 A9
B2 B4 B6 B8 B10 C1 C3 C5 C7 C9
(b)

Fig. 2 Operation voltages (a) and optical output powers (b) of the LED packages in A, B, C groups

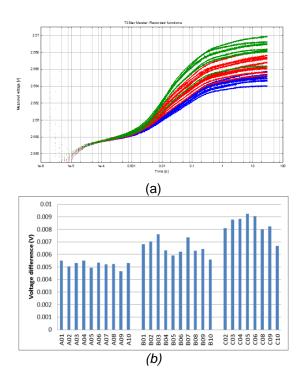


Fig. 3 Normalized operation voltages (a) and voltage differences of the LED packages in A, B, C groups

4. Conclusion

We investigated the solder-joint voids of the filp-chip LED packages using a thermal transient proposed And analysis. we an non-destructive failure screening method for flip-chip die bonding process in the LED packages. For a feasibility test, we made three groups of LED packages and analysed their thermal properties. Although, there was no difference in operation voltage and optical output power, the voltage variation in the transient region showed a good association with the bonding quality of the solder joint

References

[1] A. Hans et. al., Transient thermal analysis

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