

# Study on Failure Mechanism of Bake Unit Transfer Robot in Semi-conductor Equipment

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## 1. Introduction

Photolithography equipment performs exposing, aligning marks, and baking process on a wafer for semiconductor manufacturing. Transfer robot is a system that moves and places the wafer inside the bake unit for baking process. At a high temperature, 230°C, the baking process is finished and the transfer robot is supposed to move the wafer into the chill plate which is on a room temperature. However, it was reported that, during this process, the wafer tilts and overlaps the guide wall of the wafer on occasion. This event causes the entire manufacturing process to be stopped. The cause of the failure is not explained yet. In this study, we suggest the mechanism of the failure and perform numerical simulation and experimental test to confirm the mechanism and overcome the failure.

## 2. Failure Mechanism Investigation

When the wafer is moving up by the transfer robot, air comes in the gap between the wafer and hot plate as shown in Fig. 1. The coming air speed will depend on the speed of lifting wafer. As the geometry and air flows are symmetrical on the wafer, the pressure distribution will be symmetrical also and there is no chance to tilt the wafer during the process.

But, since there are hot and cold temperature sources, there are always air disturbance inside the bake unit. When the air disturbance is combined with the wafer lifting, the pressure distribution won't be symmetrical anymore and it is possible for the wafer to be tilted. Fluent simulations have been conducted to confirm the investigation. The results are shown in Fig. 2 for the case with and without the air disturbance. The case with air disturbance shows the unsymmetrical pressure distribution. Experimental setup is designed and test is conducted as shown in Fig. 3 to verify the failure mechanism investigation.

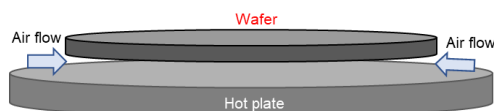


Fig.1 Inserted air flow into the wafer

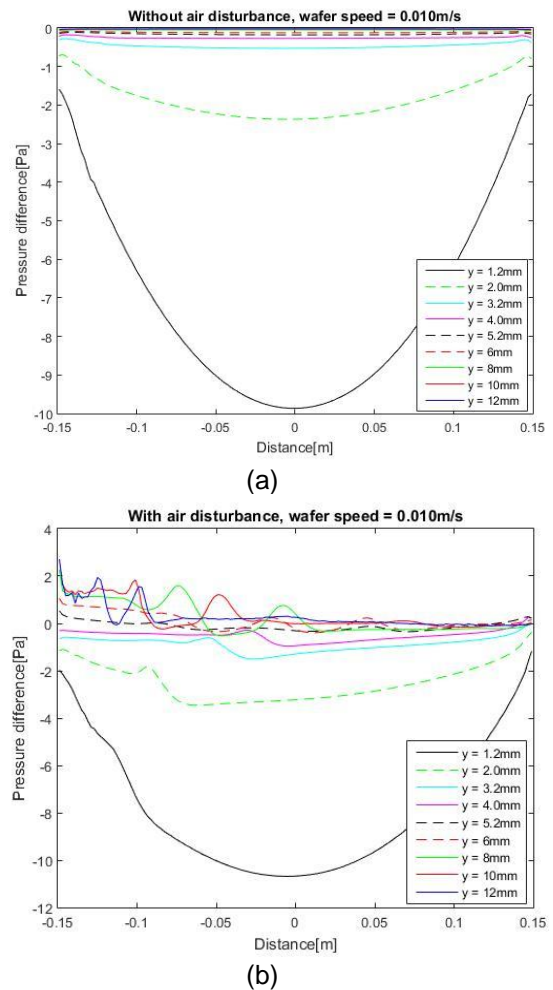


Fig.2 Simulation results of pressure difference along the wafer; (a) without and (b) with air disturbance

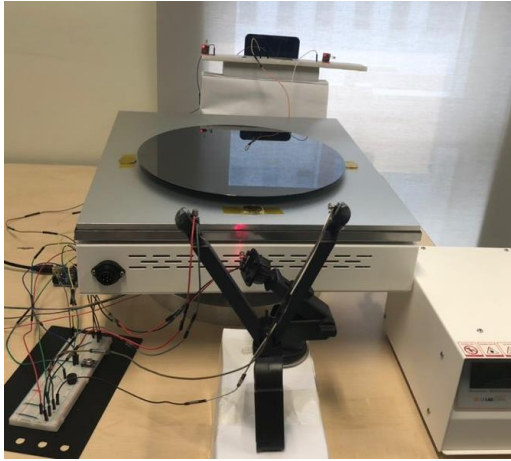


Fig.3 Experimental setup for failure mechanism verification

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